

**REMARKS**

Claims 2, 5, 7-10, 15, 19, 20-22, 27-41 and 44-50 are pending in this application, of which claims 27-33 and 39-41 have been withdrawn from consideration. Claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 have been finally rejected and are the subject of an on-going appeal to the USPTO Board of Appeals. Applicants have requested continued examination of these claims in the Request for Continued Examination filed concurrently herewith, and have amended claims 2, 5, 7, 10, 15, 18, 20, 21, 34 and 44-46. No new claims have been added.

The Examiner has maintained from the previous Office Action all of the prior art rejections of claims 2, 5, 7-10, 15, 18, 20-22, 27-41 and 44-50.

In Applicants' previous response of March 31, 2003, it was stated:

It should be noted that conductor 12 in Hiroshi, corresponding to the metallic film of the present invention, covers only the bottom surface of the resin projection. This is in contrast to the present invention as shown, for example, in Fig. 32, in which the films 113 cover both the bottom and side surfaces of the resin projections.

The Examiner has applied Atsushi for teaching this feature.

Applicants respectfully disagree. Although Atsushi discloses an optical semiconductor device in which connecting parts 6 projecting from the resin portion are completely covered by conductor pattern 2, there would be no motivation to apply this teaching to Hiroshi because conductor 12 is a flat plate covering the bottom of sealing resin 16 and the wiring board 10. There is no "projection" in Hiroshi, only the flat plate. Thus, these references may not be combined to teach the present invention.

The Examiner now argues:

In this case, the portion 1 of the Atsushi can be used to replace the bottom portion of the Hiroshi's device. This combination produces

the structure that has conductive layer which covers the bottom and the sides of the projection portion as claimed. This combination is also proper since the connections to carry the signals from the chip are made through the conductor 2.

Applicants respectfully disagree. Hiroshi utilizes a plurality of flat conductor plates 12 to provide connection from the IC element 13 to the bottom of the package in view of the intended use of the device in a plastic IC card 21 as represented in Fig. 4 of Hiroshi. In contrast, Atsushi shows four (4) projections 6 covered with a conductor pattern 2 arranged at each corner of the package, which connect the IC 3 to the bottom of the package. Thus, Atsushi utilizes projections for mounting while Hiroshi uses a plurality of flat plates for mounting. Thus, there would be no motivation for a person skilled in the art to form the projections taught by Atsushi on the flat bottom surface of the device of Hiroshi.

Furthermore, as Applicants' noted in the previous response:

Furthermore, with regard to claims 15 and 20-22, Applicants submit that the recited feature of "said resin projections extending downwards from the mount-surface and laterally extending from at least one of the resin package" is not disclosed in Hiroshi.

In the Office Action, the Examiner has urged that:

Hiroshi in fact discloses the resin profusion portions, where the bond wires 15 go through and connect to the bottom conductors. Furthermore, the resin 14 in Hiroshi is an adhesive material and can be considered as a resin tape. This resin layer performs the same function as the tape that disclosed in claim 34. The metallic layer 2 is flush with the surface as mentioned above; see also fig. 4b-5 of Atsushi.

The Examiner is incorrect and has apparently either disregarded or overlooked Applicants' argument that **Hiroshi** fails to teach the feature of resin projection projecting from the bottom surface of the device. What is disclosed in **Hiroshi** is a resin part projecting from the bottom surface of the chip, but this resin part of **Hiroshi** does not project from the bottom surface of the device. The device of **Hiroshi** has a flat bottom surface.

Furthermore, as stated in Applicants' previous response:

In regard to claim 10, **Hiroshi** discloses that connection member 14 comprising "insulative" resin. Applicants submit that this material is not the same as "resin tape."

**Hosomi et al.** has been cited for teaching the formation of metallic films 3 comprising a plurality of stacked metallic layers but, like **Hiroshi** discussed above, fails to teach, mention or suggest the electrode forming a flush surface with the package body, as recited in claim 34, from which claims 37-38 depend.

In particular, it should be noted that **Hiroshi** has an insulating substrate 11 underneath the chip. Because the resin fills the gap formed in the insulating substrate 11, there appears apparent similarity, **if the insulating substrate 11 is removed**. However, the insulating substrate 11 forms a part of the device of **Hiroshi** and cannot be removed. Thus, the device of **Hiroshi** is characterized by a flat bottom surface, contrary to the device of the present invention.

With regard to **Atsushi**, it is noted that the resin package body of **Atsushi** does have bottom projections, but the resin package body does not include the semiconductor chip therein.

Thus, Atsushi fails to teach the feature of the resin package **sealing the chip**, contrary to the present invention.

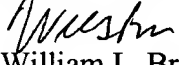
The cited references also fail to disclose that the chip is formed on a die-bonding resin layer 115, 153 or tape 173, and that the die-bonding resin layer is exposed to outside at the bottom surface of the device or at the mount-side surface, as in the present invention. Fig. 32, for example, shows this exposure which results from the removal of the lead frame, such as the lead frame 30, after the molding process.

Accordingly, the claims have been amended to recite this feature or variation of it, and the claims are now in condition for further examination.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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